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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,034	12/27/2001	Kenneth C. Creta	10559-639001 / P12351	9181

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	11

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 10/035,034	Applicant(s) CRETA ET AL.	
	Examiner Midys Inoa	Art Unit 2188	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 12 April 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *the arguments have been considered but are not persuasive*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 8-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of "The Cache Memory Book" by Jim Handy.

Regarding Claims 1-6 and 10, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") monitors which of the thirty-two portions of the storage locations have been written to. When the thirty-two-byte validity field 144 determines that all the thirty-two portions of the storage locations are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as a DCU, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of

Glew et al. and integrating a cache coherency protocol such as that of Handy. A coherency protocol would prevent the confusion between good and useless data. **In integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; however, adding the delay of a cache coherency protocol would prevent the delays caused by accessing stale data in the cache. Additionally, although Glew et al. discloses that "processor ordering is ignored", this does not mean that a coherency protocol cannot be implemented since in the case of Glew et al. a coherency protocol and processor ordering are two separate concepts. In adding a coherency protocol in the system of Glew et al. the protocol can ensure coherency between multiple microprocessors A through D (see Figure 3) and thus, processor ordering is not necessary.**

Regarding Claim 11, Glew et al. discloses an eviction mechanism for an on-chip data cache unit in which a cache line is evicted when it is determined that the cache line is full (Column 4, lines 59-67 and Column 7, lines 1-30).

Regarding Claims 8, 14, Glew et al. teaches transmitting evicted data through bus unit 130 to an external destination device, which could be a frame buffer or a separate memory (See Column 7, lines 47-52).

Regarding Claims 9, 16, Glew et al. teaches a Write Combining Unit 138 ("input/output device") which provides the data written into the storage locations of buffer 132 (See Figure 4 and Column 7, lines 15-30).

Regarding Claims 13, 15, 18, 22-26 and 28, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") being written to through the use of a write combining unit 138, and an eviction unit 139 enabled to evict data from the

storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") monitors which of the thirty-two portions of the storage locations have been written to. When the thirty-two-byte validity field 144 determines that all the thirty-two portions of the storage locations are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as a DCU, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. and integrating a cache coherency protocol such as that of Handy. A coherency protocol would prevent the confusion between good and useless data. **In integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; however, adding the delay of a cache coherency protocol would prevent the delays caused by accessing stale data in the cache. Additionally, although Glew et al. discloses that "processor ordering is ignored", this does not mean that a coherency protocol cannot be implemented since in the case of Glew et al. a coherency protocol and processor ordering are two separate concepts. In adding a coherency protocol in the system of Glew et al. the protocol can ensure coherency between multiple microprocessors A through D (see Figure**

3) and thus, processor ordering is not necessary. The system of Glew et al. initiates write transactions through an execution device 126 (Figure 3).

Regarding Claims 17 and 21, Glew et al. teaches filling cache-line size storage location with a number of combining partial writes and evicting one full storage location using a burst eviction. Therefore, if more than one write fills a storage location and only one eviction procedure evicts the same storage location, more writes must be executed for each eviction (Column 5, lines 20-33 and Column 7, lines 1-14).

Regarding Claim 19, Glew et al. does not teach using an additional write combining unit or I/O device to store additional data onto the buffer 132. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add another inputting unit to the write combining buffer of Glew et al. since such additional inputs would be integrated into the existing eviction system with ease and adding such additional inputs would give the system the ability to process more data.

Regarding Claims 12, 20 and 27, Handy discloses the workings of a MESI cache coherency protocol (pages 156-158).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of "The Cache Memory Book" by Jim Handy further in view of Van Huben et al. (2002/0083243 A1). Glew et al. in view of "The Cache Memory Book" teaches the invention as set forth by claim 1 above. Glew et al. in view of "The Cache Memory Book" does not teach evicting even if the storage location is not full, as long as there are no other evictions taking place at the same time. Van Huben et al. teaches allowing an initial LRU cast-out operation ("eviction") to complete while all other operations wait. It would have been obvious to

one of ordinary skill in the art at the time the invention was made to integrate the wait policy employed in Van Huben et al. to the invention of Glew et al. in view of "The Cache Memory Book" since such modification would prevent deadlocks or execution conflicts (pages 8-9, paragraph 112).

Response to Arguments

3. Applicant's arguments filed on April 12th, 2004 have been fully considered but they are not persuasive.

Applicant argues that Glew teaches away from coherency because in Glew's system "processor ordering is ignored for writes from the write combining buffer. No delay between consecutive partial write operations is required since global observability is no longer necessary... no read-for-ownership or similar operations need be performed to read an entire line of uncacheable data into the write combining buffer".

In integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; however, adding the delay of a cache coherency protocol would prevent the delays caused by accessing stale data in the cache. Additionally, although Glew et al. discloses that "processor ordering is ignored", this does not mean that a coherency protocol cannot be implemented since in the case of Glew et al. a coherency protocol and processor ordering are two separate concepts. In adding a coherency protocol in the system of Glew et al. the protocol can ensure coherency between multiple microprocessors A through D (see Figure 3) and thus, processor ordering is not necessary.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

Kevin L. Ellis
Primary Examiner